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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/857,779	07/26/2001	Masahiro Oohashi	HYAE:119	9768

7590 05/18/2004  
Parkhurst & Wendel  
1421 Prince Street Suite 210  
Alexandria, VA 22314-2805

EXAMINER

RAO, ANAND SHASHIKANT

ART UNIT	PAPER NUMBER
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2613

DATE MAILED: 05/18/2004

10

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/857,779

Applicant(s)

OOHASHI ET AL.

Examiner

Andy S. Rao

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 2/12/02.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 5.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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## **DETAILED ACTION**

### ***Specification***

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "first arithmetic block", "second arithmetic block", "first arithmetic block" "third arithmetic block" "fourth arithmetic block", "fifth arithmetic block", "sixth arithmetic block", "seventh arithmetic block", "eighth arithmetic block", and "above-described arithmetic block" in lines 9-14. There is insufficient antecedent basis for this limitation in the claim.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Fu et al.,  
(hereinafter referred to as "Fu").

Fu discloses a deblocking filter arithmetic apparatus (Fu: figures 18-19), comprising: a first through eighth arithmetic blocks which receive (Fu: column 21, lines 55-67; column 22, lines 1-30), respectively, as inputs simultaneously every two adjacent data among a first to an eighth pixel data (Fu: column 21, lines 7-15), carry out one of the cycles of the processing arithmetic constituting the filtering processing corresponding to first to eighth pixel data (Fu: column 21, lines 21-30) and performed for the removal of block noises (Fu: column 9, lines 45-57), every time two of the pixel data are input, and output the respective pixel data having been subjected to the filtering processing (Fu: column 21, lines 40-47), being providing in parallel corresponding to the first to the eight pixel data and to which two of the pixel data are input simultaneously (Fu: column 20, lines 55-67); an output selection circuit which selects one from the outputs from the first to the eighth arithmetic blocks and outputs the same (Fu: column 18, lines 48-57); and a control circuit which controls the processing arithmetic of each arithmetic block (Fu: column 20, lines 3-25), in accordance with the cycles of the processing arithmetic, so that the cycles of the processing arithmetic performed in each combination, among a combination of the first and second arithmetic block, a combination of the third and fourth arithmetic block, a combination of the fifth and six arithmetic block, and a combination of the seventh and eight arithmetic block (Fu: column 22, lines 30-67; column 21, lines 1-15), respectively constituted by above described arithmetic blocks up to the conclusion of the filtering processing of each combination should be concluded in an order successively among the

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respective combinations (Fu: column 21, lines 35-47), and which controls the output of the selection circuit so as to select the output from the arithmetic blocks in a unit of the combination of the arithmetic blocks and to perform a pipeline output (Fu: column 27, lines 60-67; column 28, lines 40-50), as claim 1.

Regarding claim 2, Fu discloses that the arithmetic block comprises a first selection circuit, a second selection circuit, a third selection circuit (Fu: column 21, lines 1-10), a first, second shifter, an adder as specified, a register, and a third shifter (Fu: column 21, lines 20-47), as in the claim.

Fu discloses a deblocking filter arithmetic apparatus (Fu: figures 18-19), comprising: a step for receiving (Fu: column 21, lines 55-67; column 22, lines 1-30), respectively, as inputs simultaneously every two adjacent data among a first to an eighth pixel data (Fu: column 21, lines 7-15), carry out one of the cycles of the processing arithmetic constituting the filtering processing corresponding to first to eighth pixel data (Fu: column 21, lines 21-30) and performed for the removal of block noises (Fu: column 9, lines 45-57), so that the cycles of the processing arithmetic performed in each combination, among a combination of the first and second arithmetic block, a combination of the third and fourth arithmetic block, a combination of the fifth and six arithmetic block, and a combination of the seventh and eight arithmetic block (Fu: column 22, lines 30-67; column 21, lines 1-15), respectively constituted by above described arithmetic blocks up to the conclusion of the filtering processing of respective combinations should be concluded in an order successively (Fu: column 21, lines 35-47); and a step for performing a pipeline output of pixel data which are obtained by the above-described step with

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having been subjected to the filtering processing, for the respective combinations of the pixel data in an order successively (Fu: column 27, lines 60-67; column 28, lines 40-50), as claim 3.

### *Conclusion*

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gonzales discloses a process pipeline architecture for image/video processing. Mandavilli discloses instructions for arithmetic operations on vectored data. Schultz discloses a system for maintaining datastream continuity. Cooper discloses a spatial scan replication circuit. Tran discloses a fast lapped image transform using lifting steps. Tan discloses a technique for minimizing decision feedback equalizer wordlength in the presence of a DC compoment.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy S. Rao whose telephone number is (703)-305-4813. The examiner can normally be reached on Monday-Friday 8 hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris S. Kelley can be reached on (703)-305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Andy S. Rao  
Primary Examiner  
Art Unit 2613

ANDY RAO  
PRIMARY EXAMINER

asr

May 7, 2004